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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,827	02/09/2004	Rolf Weis	02P15178US/INTECH 3.0-079	9772

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SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 12/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,827	WEIS ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-44* is/are pending in the application.

4a) Of the above claim(s) *1-6 and 13-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's election filed October 19, 2005. Claims 1-44 are pending. Claims 7-12 are elected without traverse as treated.

Election/Restrictions

1. Applicant's election filed October 19, 2005 of claims 7-12 is acknowledged. The election is implicitly "without traverse", and has been also treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 1-6,13-44 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

3.

Specification

4. Specification line 11 of paragraph [0041], "contacts 80 (shown in Figure 6H)" should be --contacts 81 (shown in Figure 6H)--. Appropriate correction is required.

5.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

7. Claims 7-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Arnold et al (2004/0238868).

Re claim 7, Arnold teaches (at Figures 1-7,14C-21; paragraphs 40-90) a memory cell for a memory cell array comprised of a plurality of the memory cells arranged in rows and columns (Figs 1A,2,3,7,14C-21C) the memory cell comprising: at least two deep trench structures 20

(Fig 2; paragraphs 45-51) formed in a semiconductor substrate, at least one of the deep trench structures being in electrical contact with a buried strap region 28 formed in the substrate that adjoins the at least one deep trench structure; and at least one isolation trench 10 adjoining the two deep trench structures (Figs 2,3), the one isolation trench being inherently defined using a mask comprised of a lines and spaces pattern such that at least one active area 6 is defined by the isolation trench 10 (Fig 3) and by the buried strap region 28, the active area 6 including the buried strap region 28 , each of the lines and spaces extending across the memory cell array (Figs 1A,2,3,7,14C-21C; paragraphs 45-51;84-90), wherein a plurality of isolation trenches, bit lines, and word lines in lines and spaces are formed on the semiconductor substrate (Figs 7,2,3,14C), wherein with respect to the use of a masking layer comprising lines and spaces, a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). Re claim 8, wherein the at least two deep trench structures 20 are separated by a distance 3F, where F is a minimum feature size (see Fig 2). Re claim 9, wherein the at least one deep trench structure comprises: a deep trench 20 formed within a semiconductor substrate; a buried plate region 26 adjoining a bottom region of the at least one deep trench 20 within the semiconductor substrate; a dielectric film 29 formed along sidewalls of the deep trench, an upper region of a portion of the dielectric film being removed such that a trench collar 30 is formed along a middle portion of a side of the deep trench 20 (Figs 2,3 4A-4E; paragraphs 52-57), the portion of the dielectric film being defined by a patterned masking layer such that a further portion of the dielectric film is covered by the masking layer and the portion of the dielectric is exposed; the deep trench being at least partly filled with doped polysilicon 54, the dopants in the polysilicon diffusing through the side of the deep trench into an adjoining region of the semiconductor substrate to form the buried strap region 28 align the side of the deep trench 20. Re claim 10, wherein openings in the masking layer have a pitch equal to twice a minimum feature size in the memory cell, the openings in the masking layer exposing a common region of the dielectric film in each of the plurality of the memory cells, the buried strap region 28 of each of the plurality of the memory cells adjoining a same side of the deep trenches 20 (Figs 2-3), wherein with respect to the use of a masking layer comprising openings in the masking layers having a pitch as recited, a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15

at 17 (footnote 3). Re claim 11, wherein openings in the masking layer have a pitch equal to four times that of a minimum feature size in the memory cell, the openings in the masking layer exposing opposing regions of the dielectric film in adjacent ones of the plurality of the memory cells, the buried strap region of the adjacent ones of the plurality of the memory cells adjoining opposite side of its deep trenches, wherein with respect to the use of a masking layer comprising openings in the masking layers having a pitch as recited, a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). Re claim 12, further comprising: a trench top oxide layer 32 formed atop of the doped polysilicon 54 in the at least one deep trench 20 (Fig 4C); a gate dielectric layer 36(Figs 2,4C) formed on the side of the deep trench 20; the deep trench being filled with a further polysilicon 34 layer atop the trench top oxide layer 32; a doped region 38 (2,3,6C) formed in a top surface of the semiconductor substrate adjacent to the gate dielectric layer; a contact region to the further polysilicon layer that connects the further polysilicon layer to a word line; and another contact region to the doped region that connects the dope region to a bit line (Figs 2-3; 6C-6I).

A "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Applicant has the burden of proof in such cases, as the above caselaw makes clear.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-18

Michael Trinh
Primary Examiner